

FIG.1

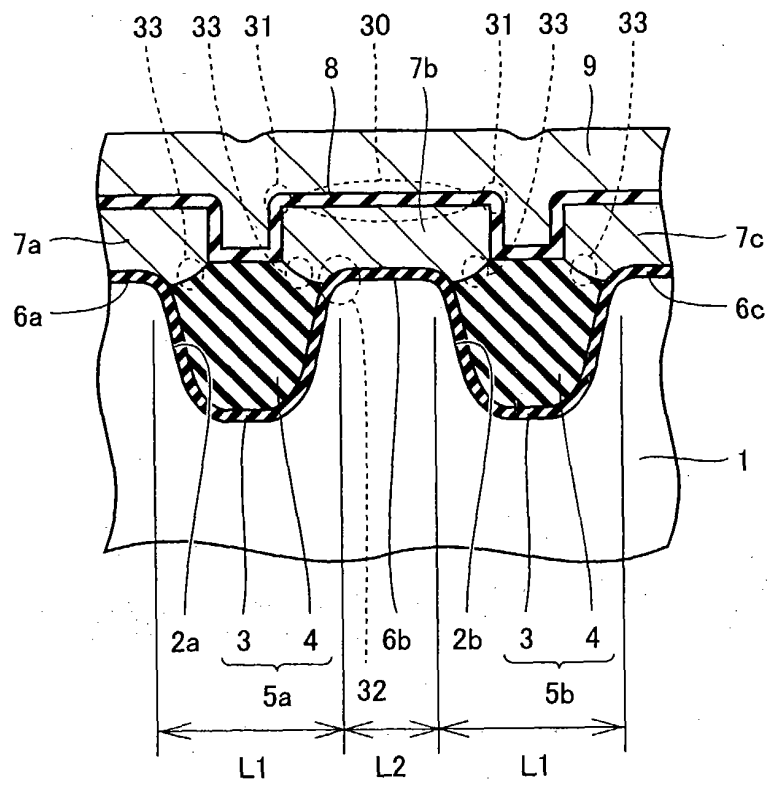


FIG.2

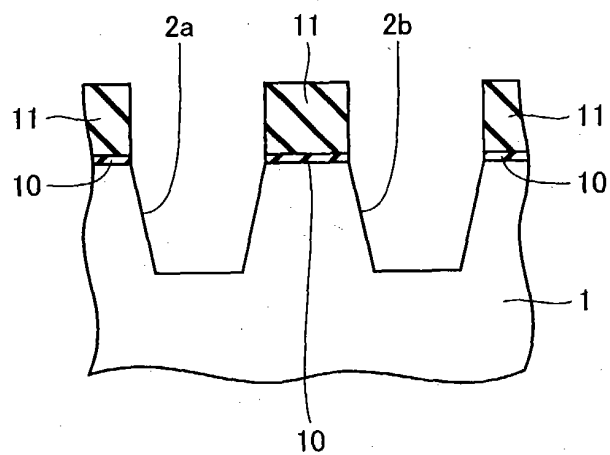


FIG.3

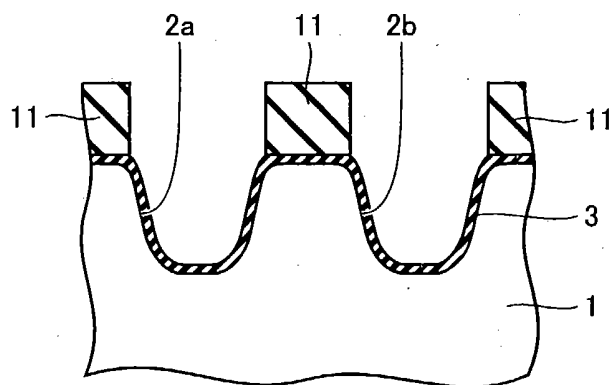


FIG.4

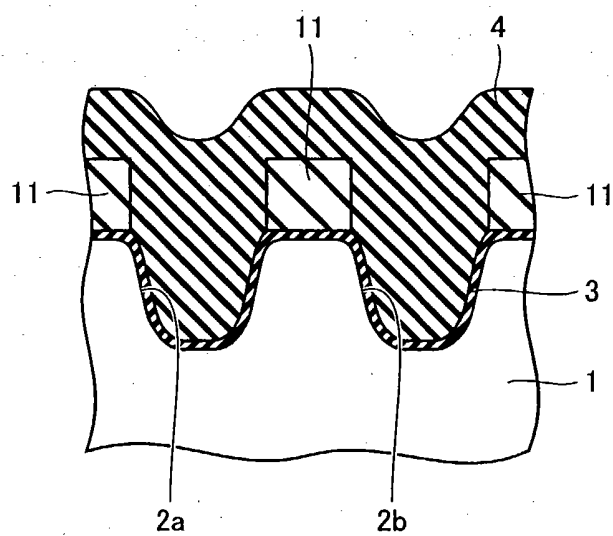


FIG.5

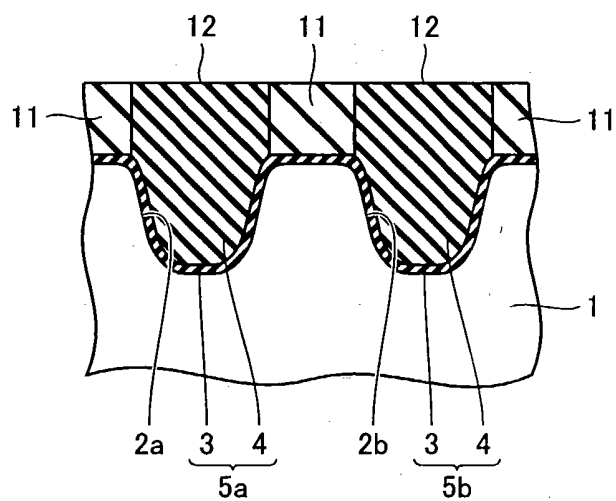


FIG.6

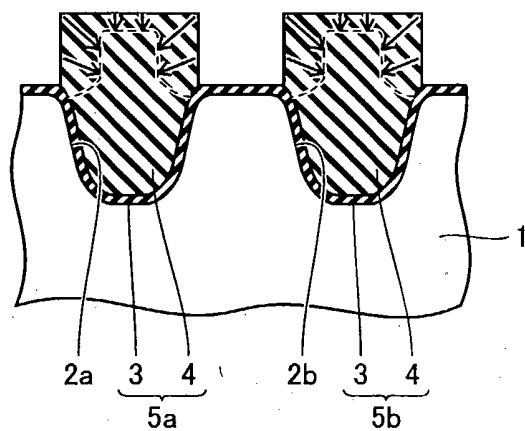


FIG.7

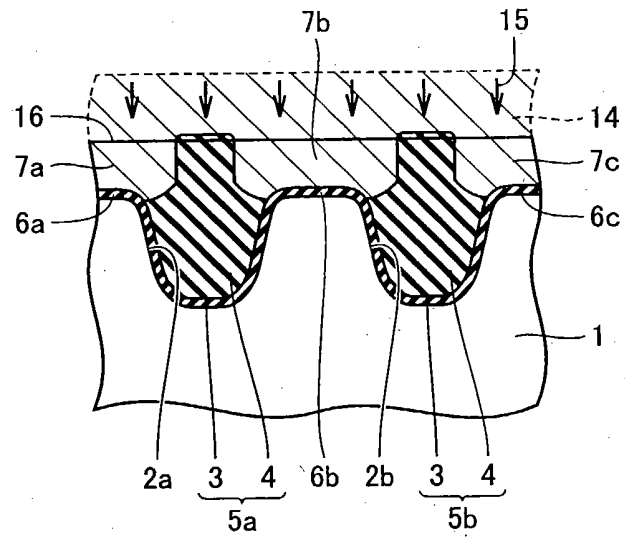


FIG.8

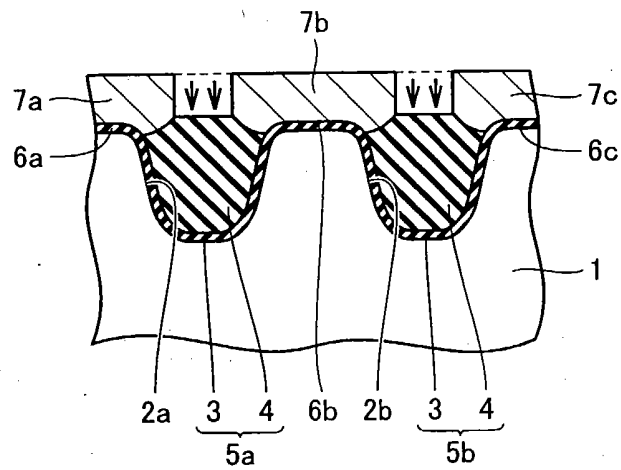


FIG.9

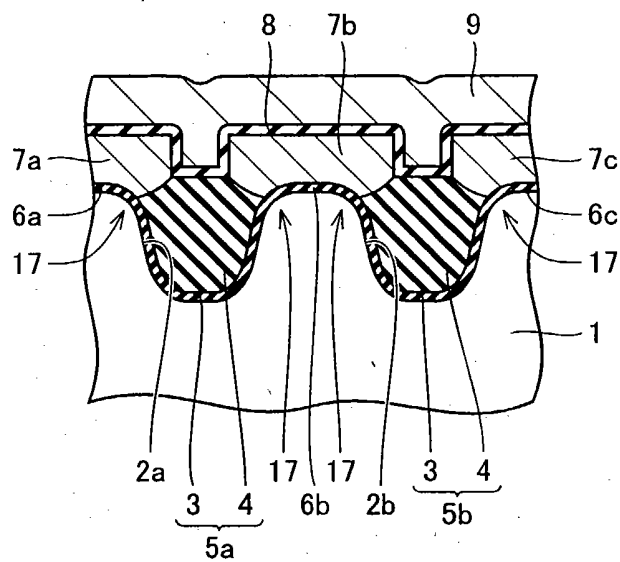


FIG.10

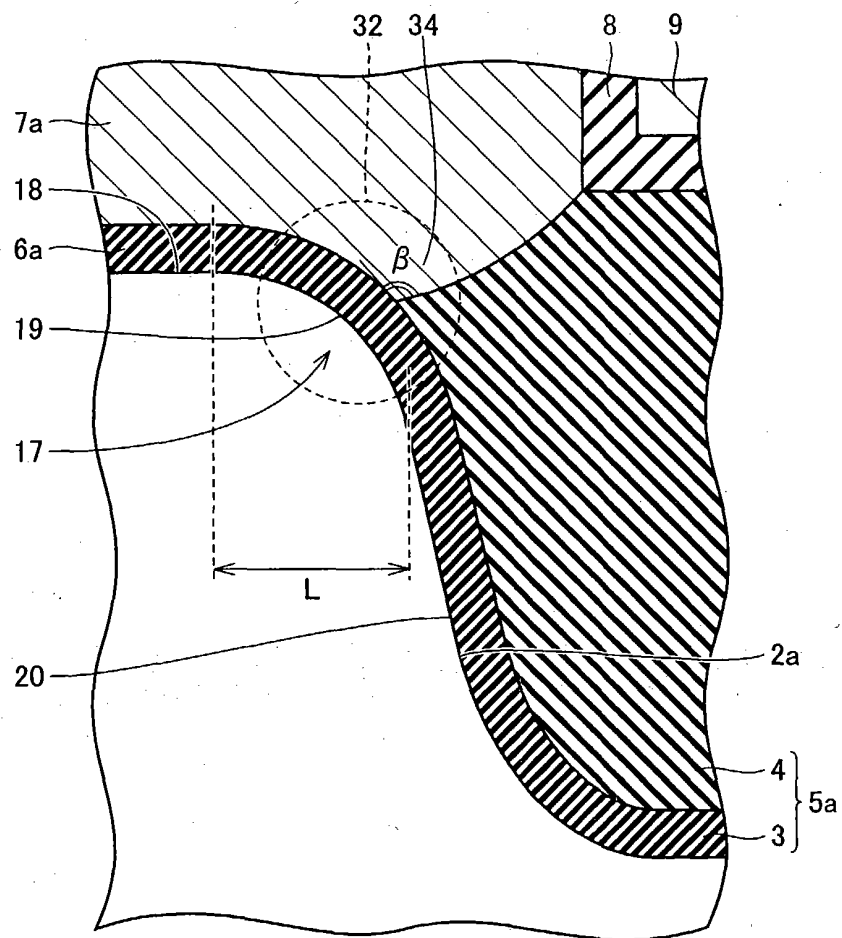


FIG.11

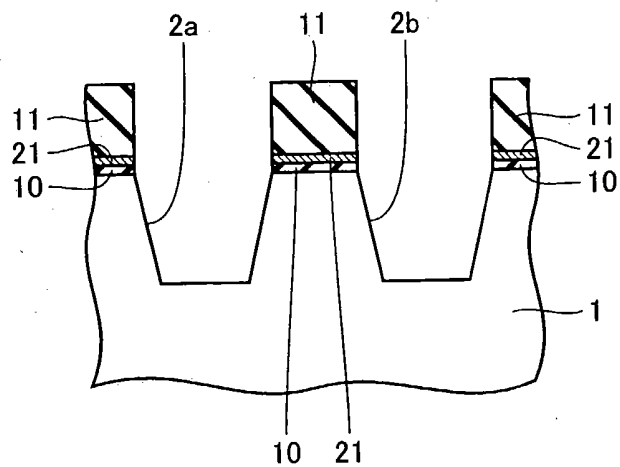


FIG.12

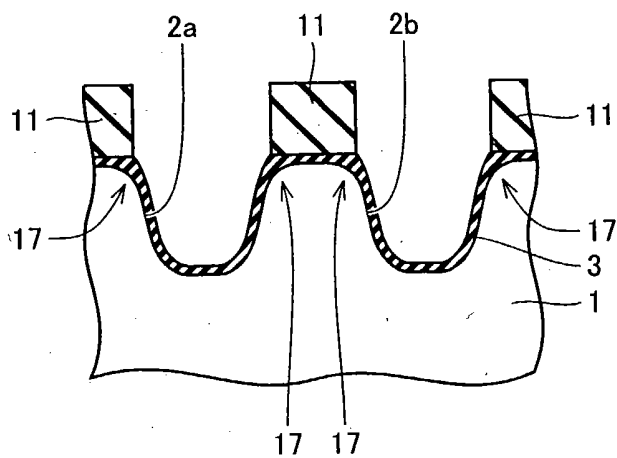


FIG.13

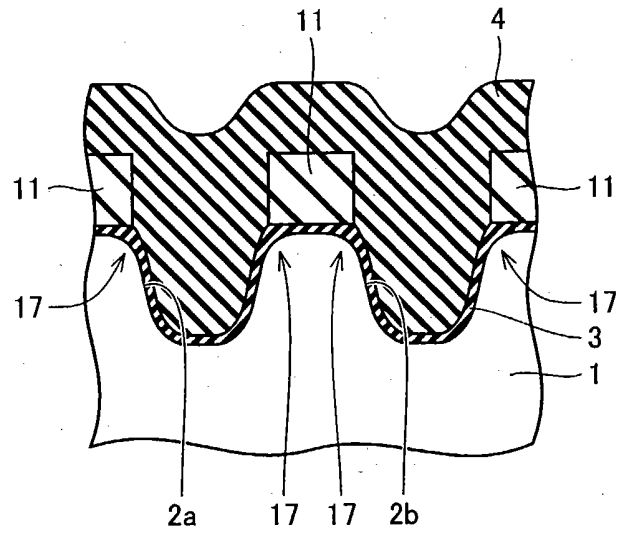


FIG.14

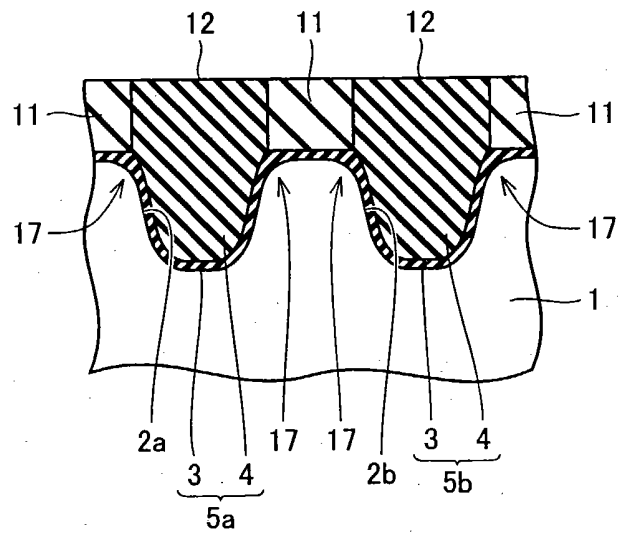




FIG.15

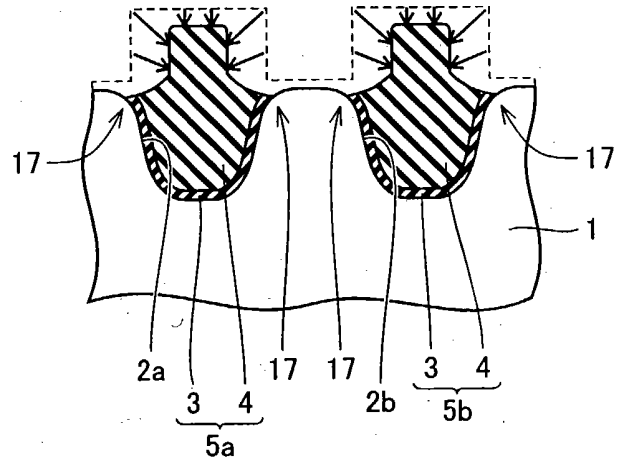


FIG.16

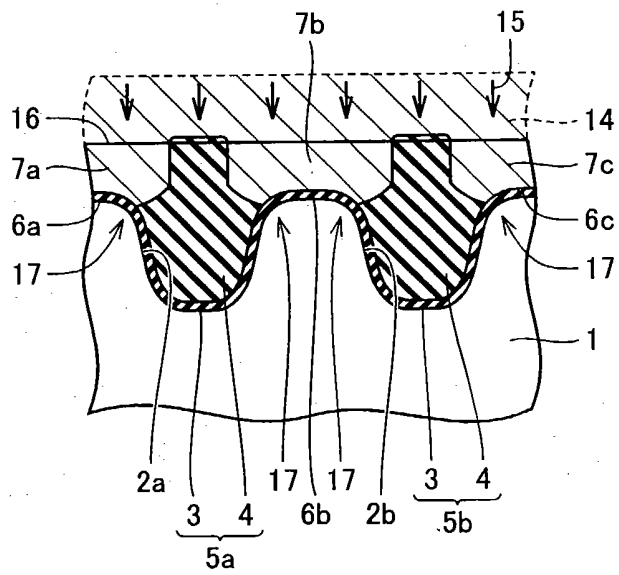


FIG.17

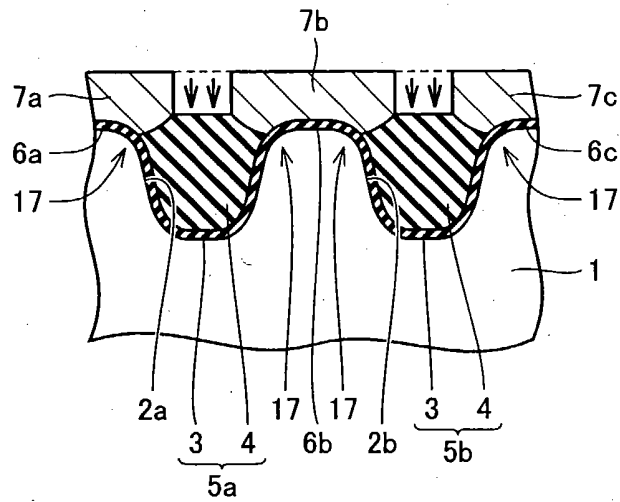


FIG.18

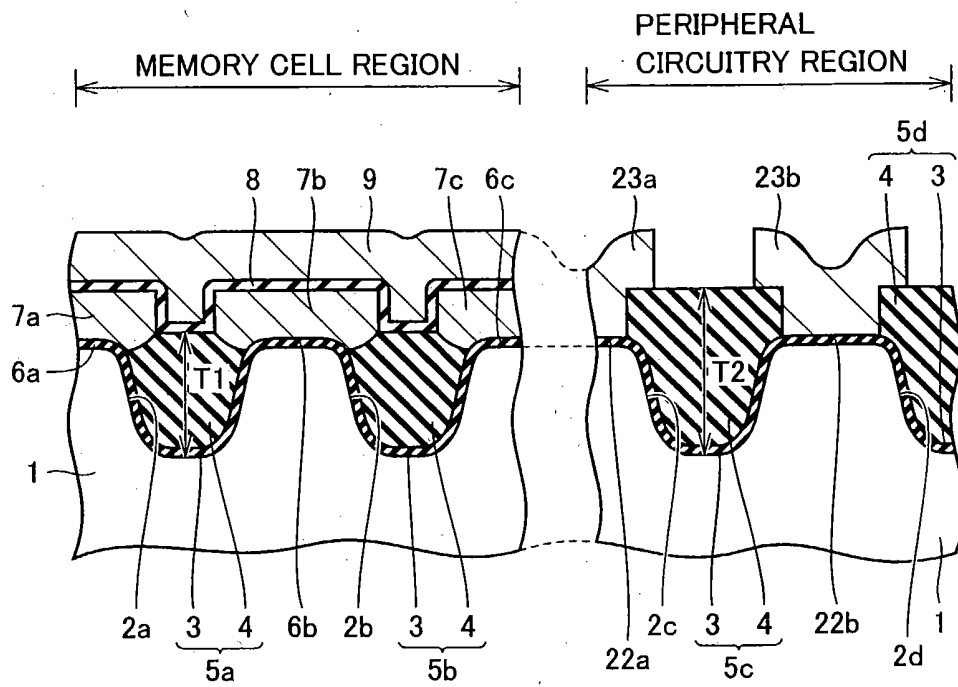


FIG.19

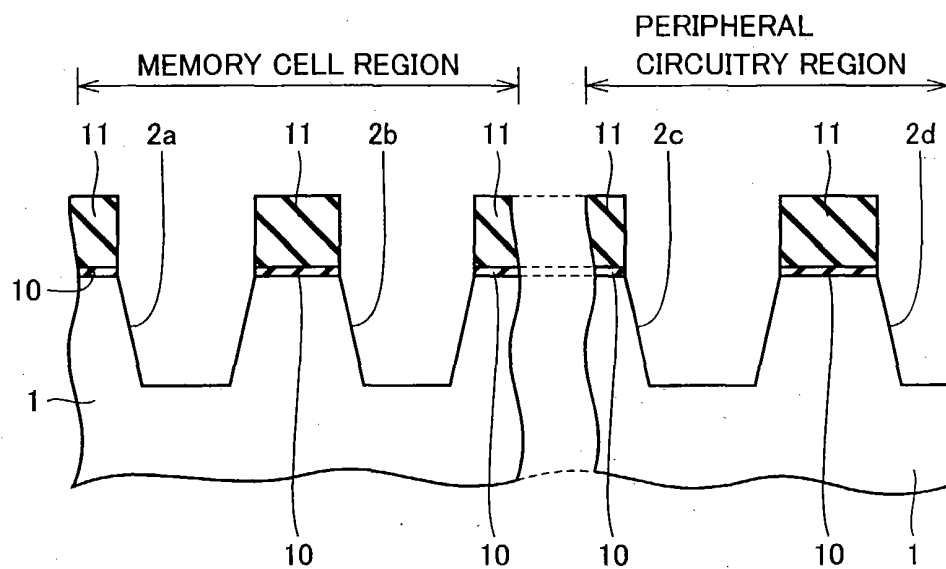


FIG.20

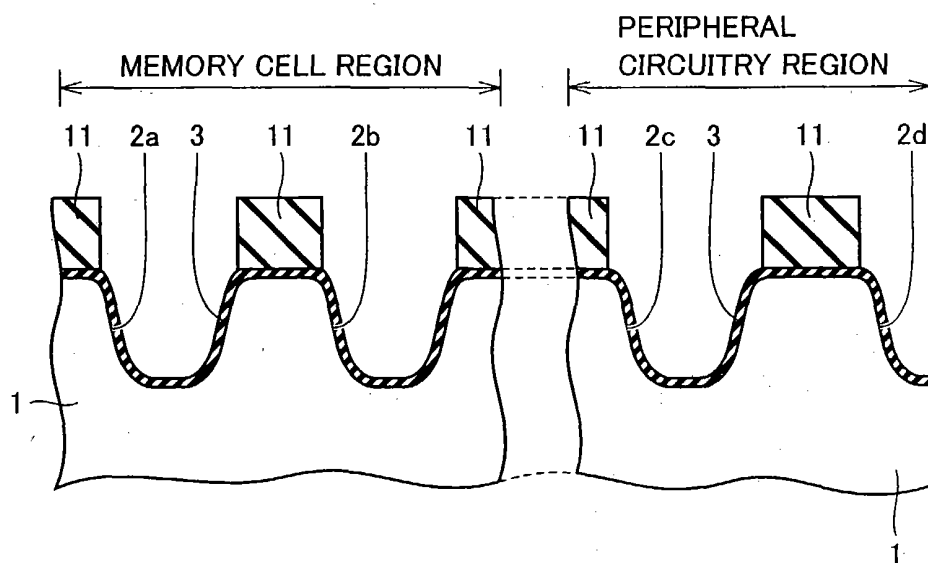


FIG.21

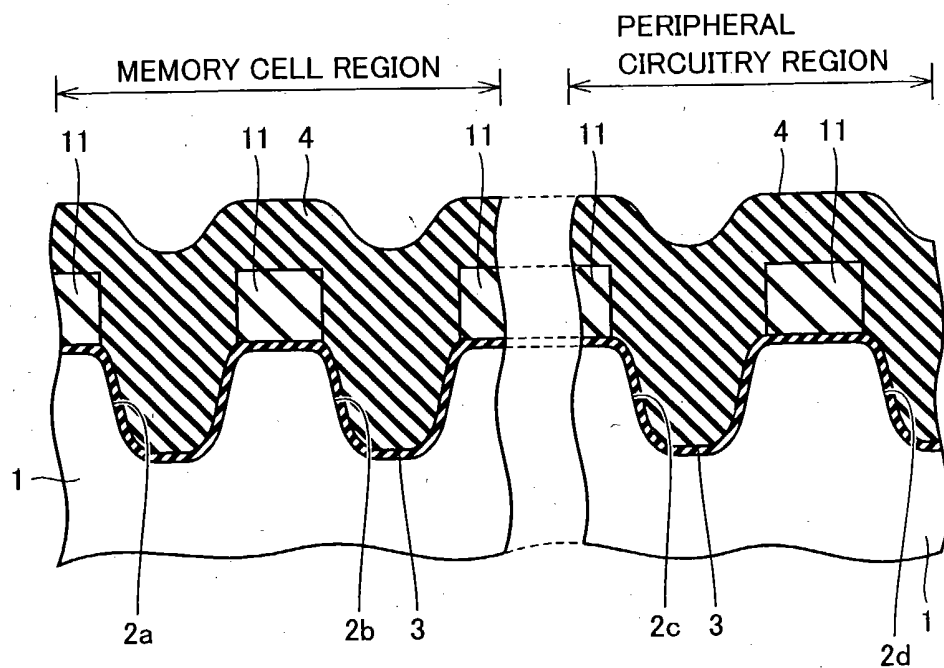


FIG.22

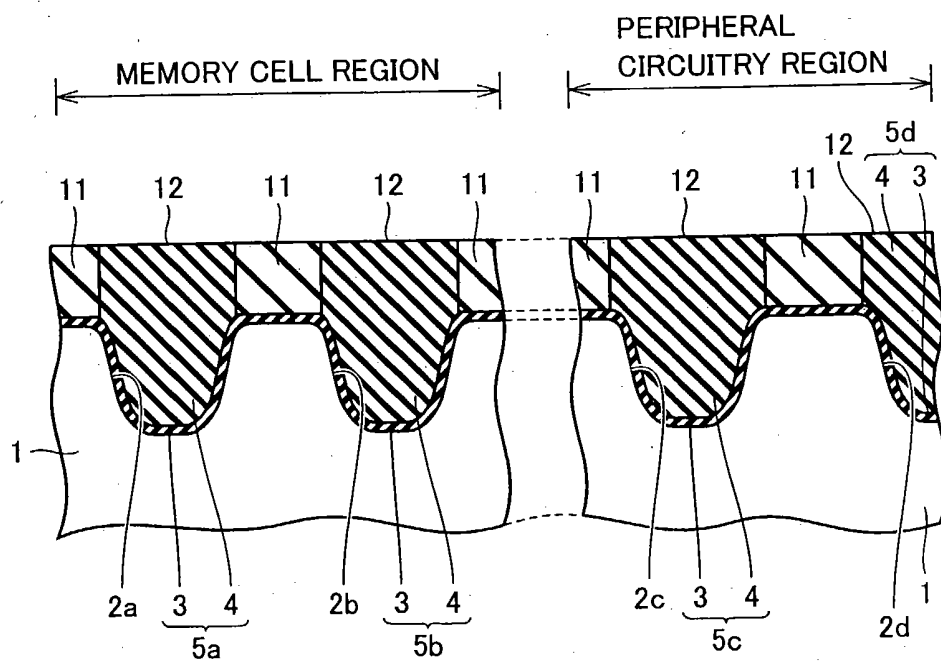


FIG.23

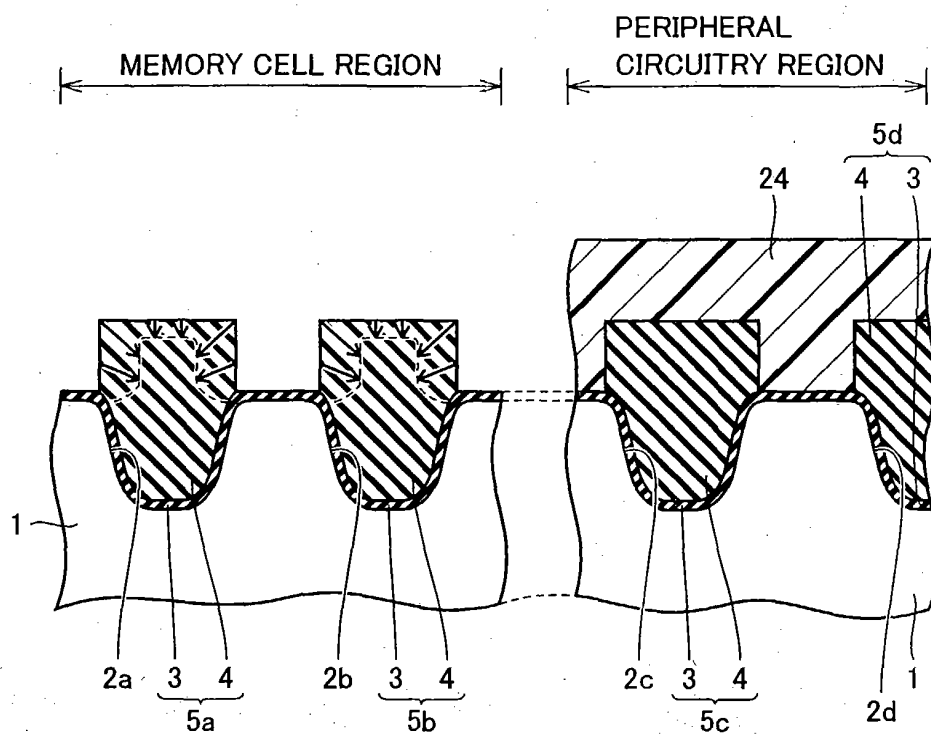
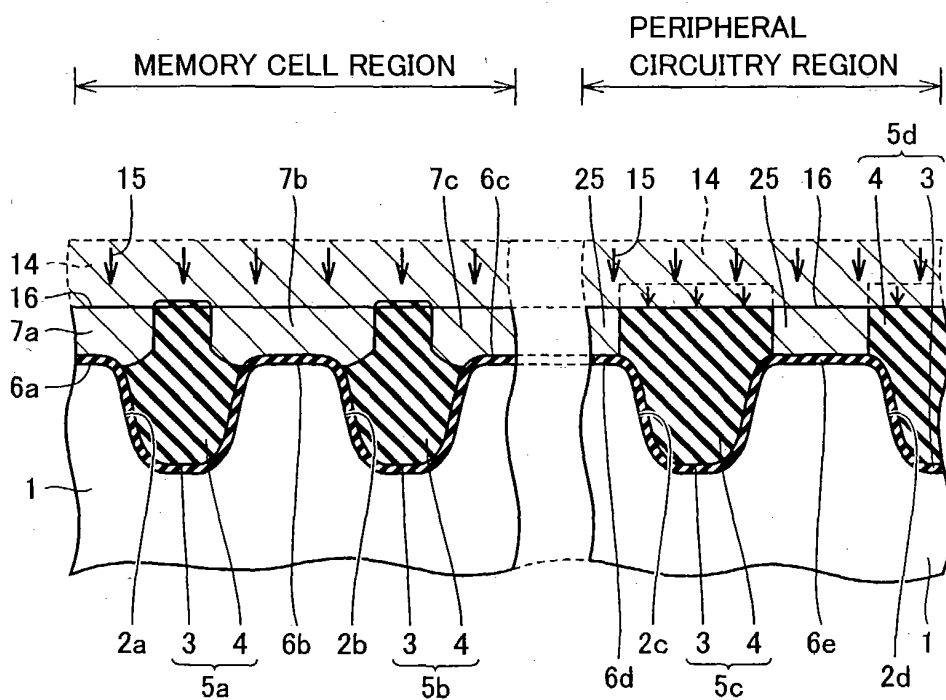


FIG.24



The diagram is a cross-sectional view of a semiconductor device, divided into two main sections: the **MEMORY CELL REGION** on the left and the **PERIPHERAL CIRCUITRY REGION** on the right. A dashed vertical line separates the two regions.

**Memory Cell Region:** This region contains two memory cells. Each cell consists of a **word line** (labeled 7a, 7b, 7c) and a **bit line** (labeled 6a, 6b, 6c). The word lines are horizontal, and the bit lines are vertical. The memory cells are formed by the intersection of these lines, creating a grid pattern. The cells are labeled 2a, 3, 4, 5a, 6b, 2b, 3, 4, 5b, and 1.

**Peripheral Circuitry Region:** This region contains peripheral circuitry, including a **word line** (labeled 25, 24, 25) and a **bit line** (labeled 4, 3). The word lines are horizontal, and the bit lines are vertical. The peripheral circuitry is formed by the intersection of these lines, creating a grid pattern. The peripheral circuitry is labeled 25, 24, 25, 4, 3, 5d, 6d, 2c, 3, 4, 5c, 6e, 2d, and 1.

The diagram illustrates the layout and structure of the device, showing the relationship between the memory cells and the peripheral circuitry. The labels 1, 2a, 3, 4, 5a, 6b, 2b, 3, 4, 5b, 1, 25, 24, 25, 4, 3, 5d, 6d, 2c, 3, 4, 5c, 6e, 2d, and 1 are used to identify specific components and regions within the device.

The diagram illustrates a cross-sectional view of a semiconductor device, divided into two main functional areas: the MEMORY CELL REGION and the PERIPHERIAL CIRCUITRY REGION.

**MEMORY CELL REGION:** This region contains three repeating memory cell structures. Each structure consists of a central gate stack (labeled 7a, 7b, 7c) and side gates (labeled 6a, 6b, 6c). The gate stacks are separated by spacers (labeled 8). The side gates are connected to a common source/drain region (labeled 1). The source/drain regions are formed in a substrate (labeled 2a, 2b, 2c) and are covered by a passivation layer (labeled 3). The passivation layer is patterned to form openings (labeled 4) for electrical contacts (labeled 5a, 5b, 5c).

**PERIPHERIAL CIRCUITRY REGION:** This region contains a peripheral circuit structure. It features a gate stack (labeled 25) and side gates (labeled 8). The side gates are connected to a common source/drain region (labeled 1). The source/drain regions are formed in a substrate (labeled 2d) and are covered by a passivation layer (labeled 3). The passivation layer is patterned to form openings (labeled 4) for electrical contacts (labeled 5d).

The diagram shows the detailed structure of the device, including the gate stacks, side gates, source/drain regions, passivation layer, and electrical contacts. The labels 1 through 8 and 25 identify the various components of the device.

[illegible]

The diagram illustrates a cross-sectional view of a semiconductor device, divided into two main functional areas: the MEMORY CELL REGION on the left and the PERIPHERAL CIRCUITRY REGION on the right. The device is built on a substrate (1). In the memory cell region, the device features a series of repeating memory cells. Each cell includes a gate stack (8) on top of a channel region (9). The channel region is defined by side walls (7a, 7b, 7c) and a bottom layer (6a, 6b, 6c). The gate stack is composed of a gate oxide (7a) and a gate electrode (7b). The channel region is formed by a channel oxide (6a) and a channel layer (6b). The device also includes a source/drain region (2a, 2b, 2c) and a contact layer (3, 4). The peripheral circuitry region contains a larger gate stack (9) and a contact layer (4, 3). The device is further divided into regions 5a, 5b, and 5c, which are defined by the gate stack and the channel region. The regions 5a and 5b are located under the memory cells, while region 5c is located under the peripheral circuitry. The regions 5a and 5b are further divided into sub-regions 2a, 3, 4, 6b, 2b, 3, 4, and 22a, 2c, 3, 4, 22b, 2d, 1, respectively. The regions 5a and 5b are also labeled with 5a and 5b, respectively. The regions 5c and 5d are also labeled with 5c and 5d, respectively. The regions 5a and 5b are also labeled with 5a and 5b, respectively. The regions 5c and 5d are also labeled with 5c and 5d, respectively.

FIG.29

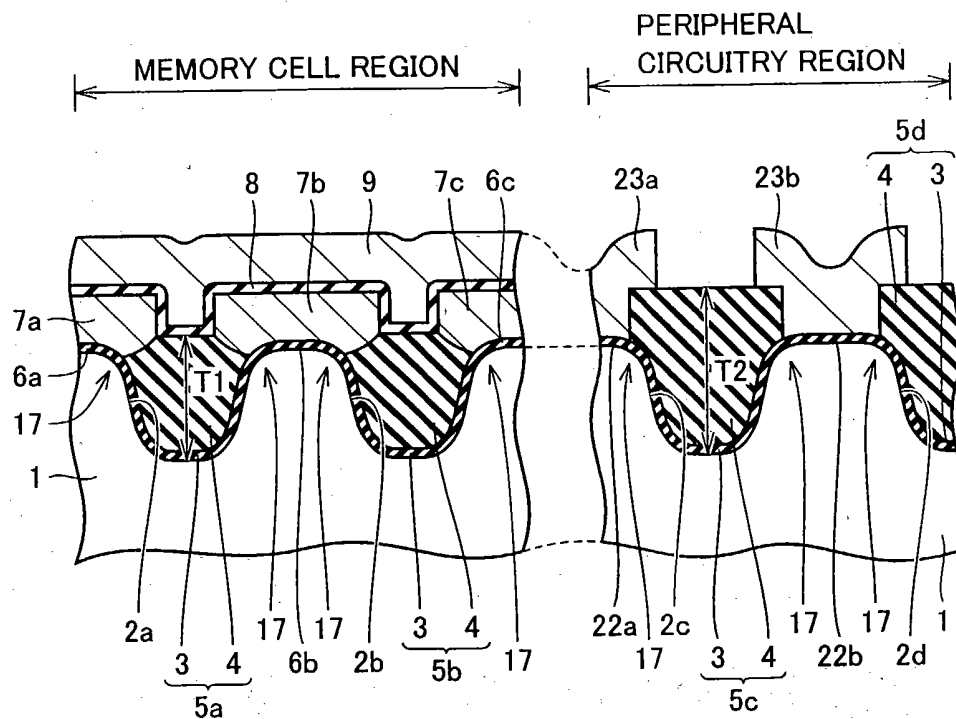


FIG.30

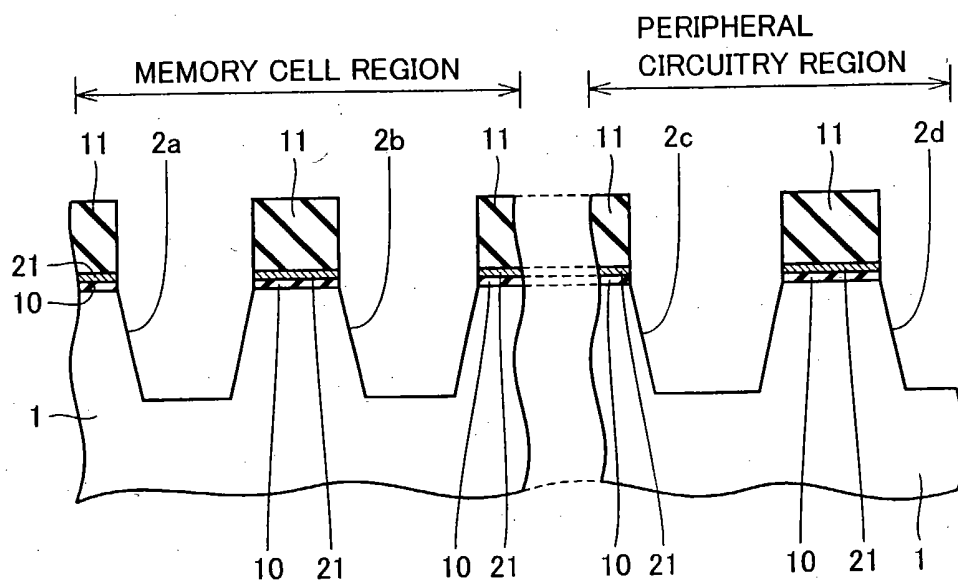




FIG.31

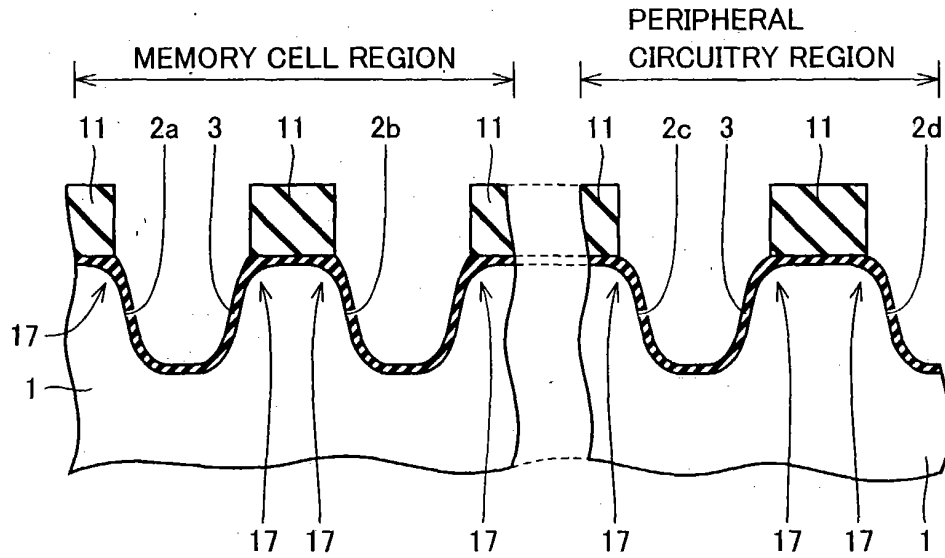


FIG.32

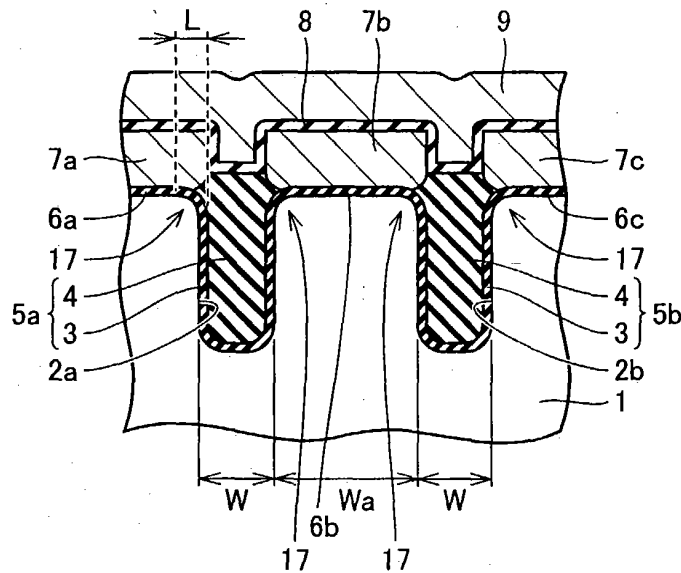


FIG.33

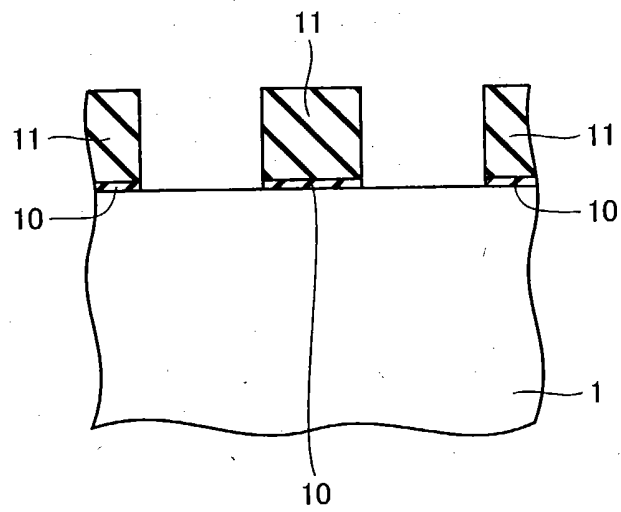


FIG.34

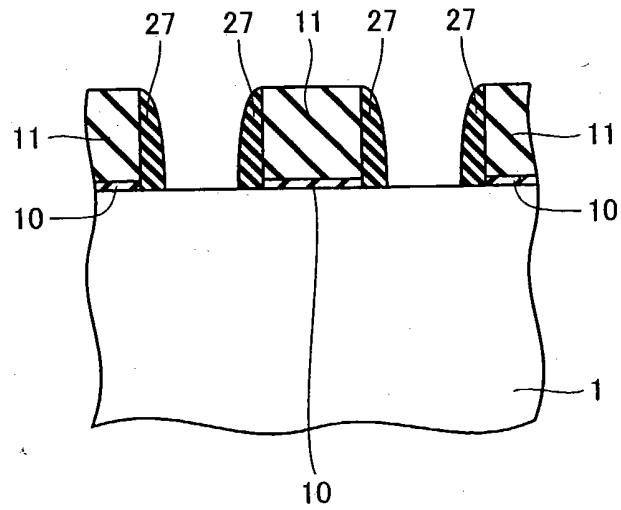


FIG.35

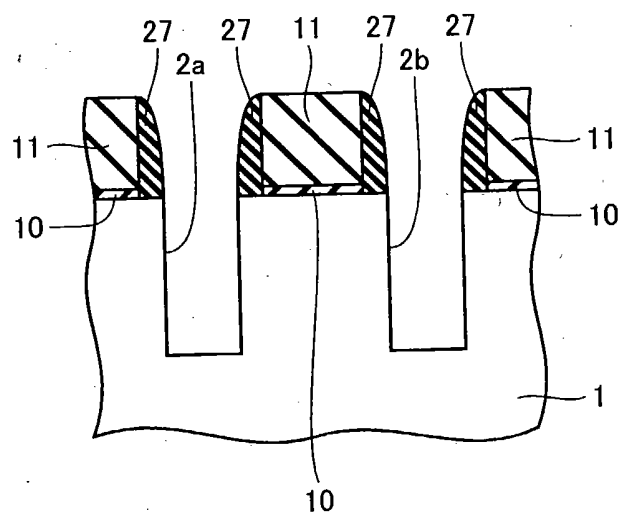


FIG.36

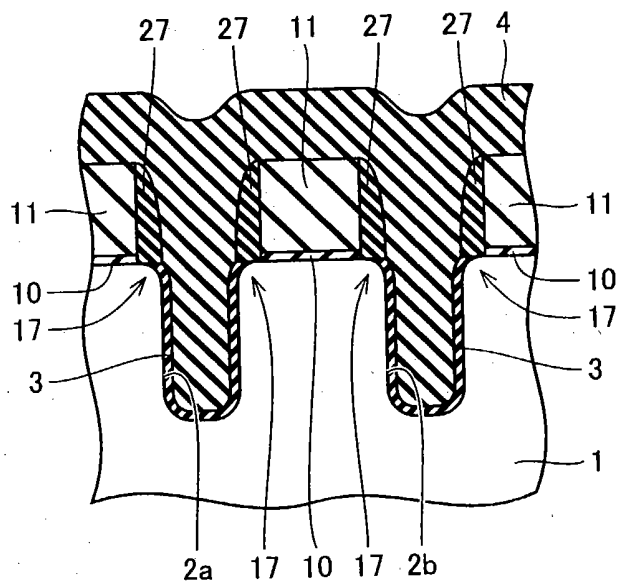


FIG.37

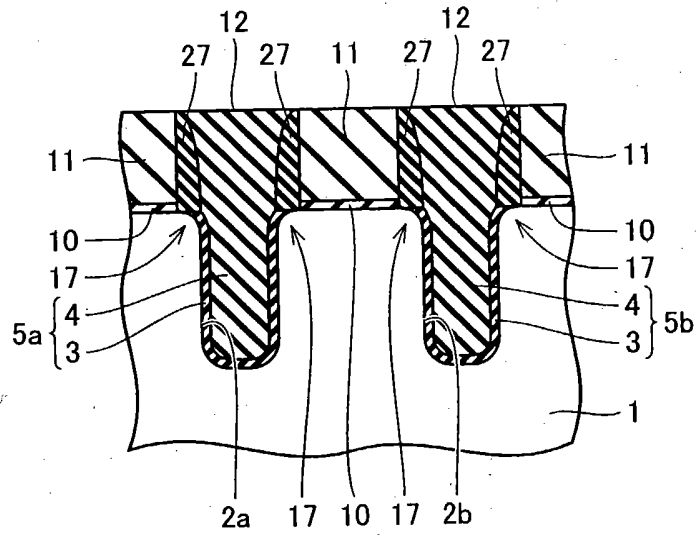


FIG.38

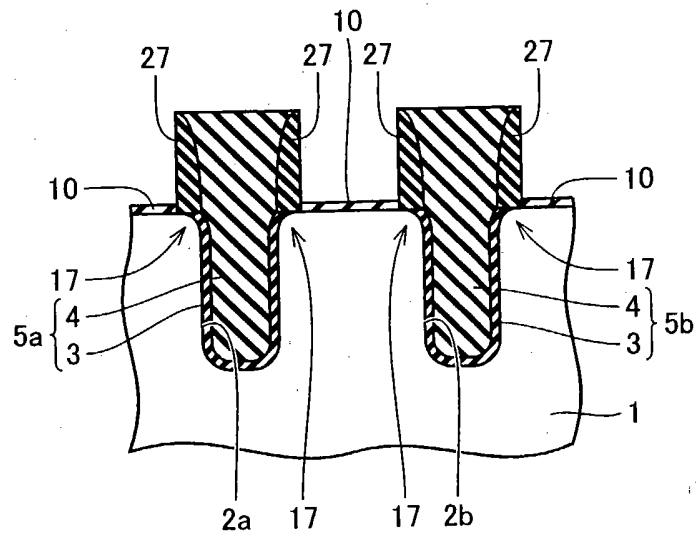


FIG.39

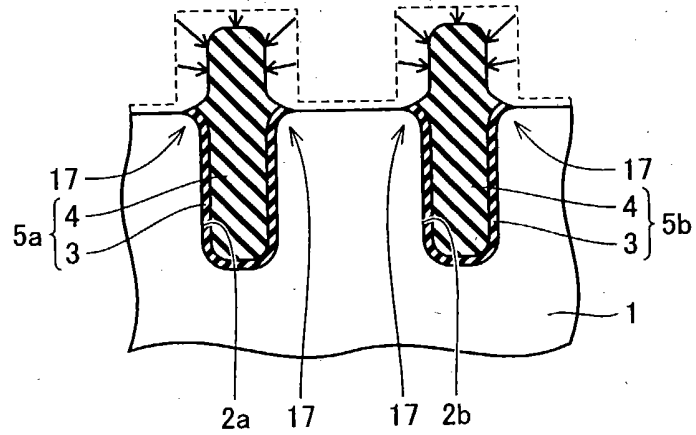


FIG.40

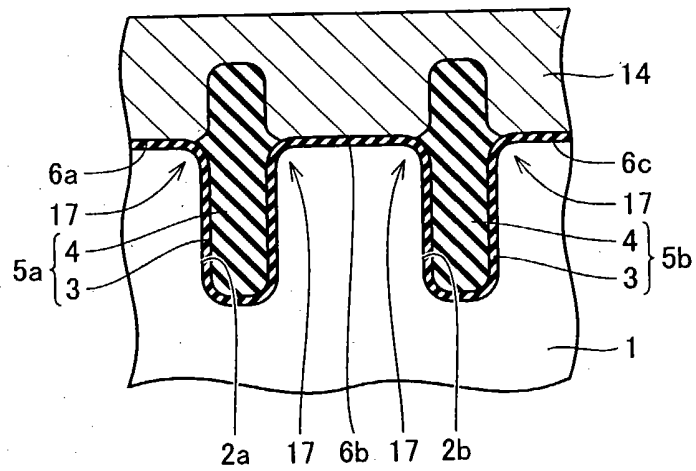


FIG.41

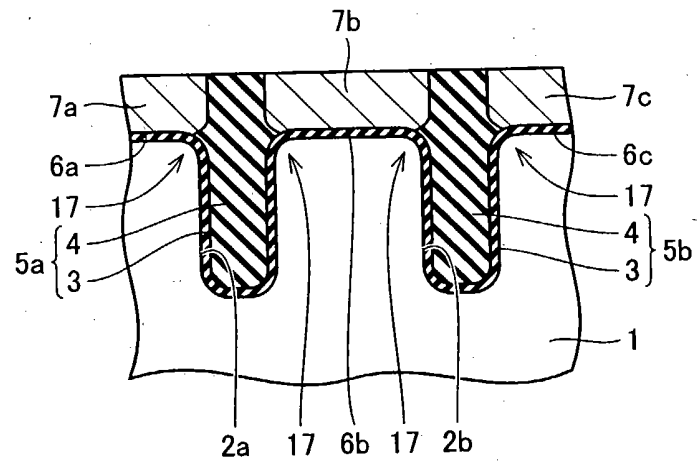


FIG.42

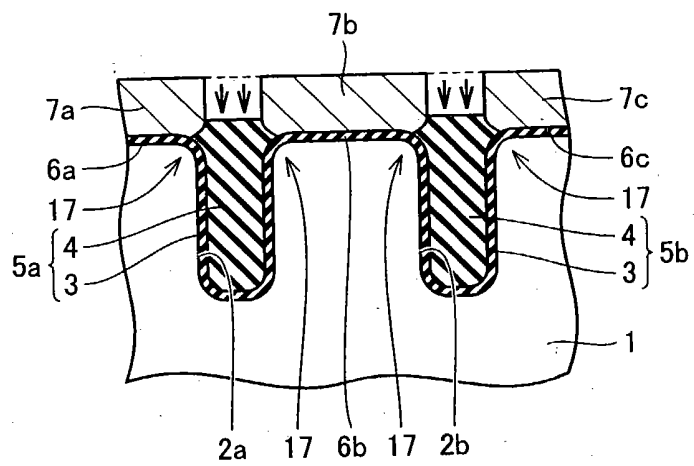


FIG.43

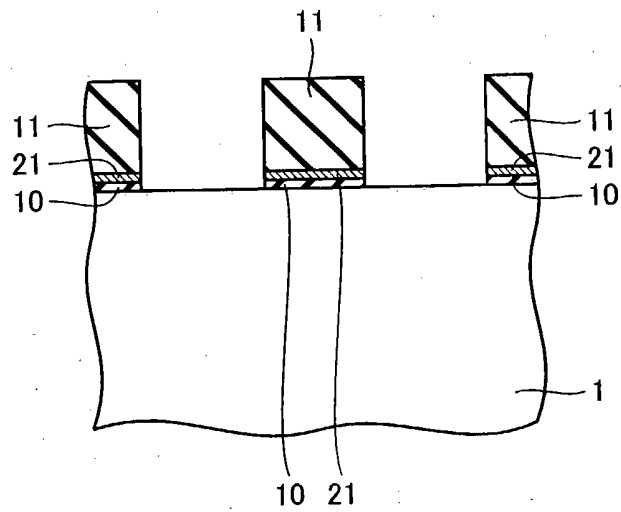


FIG.44

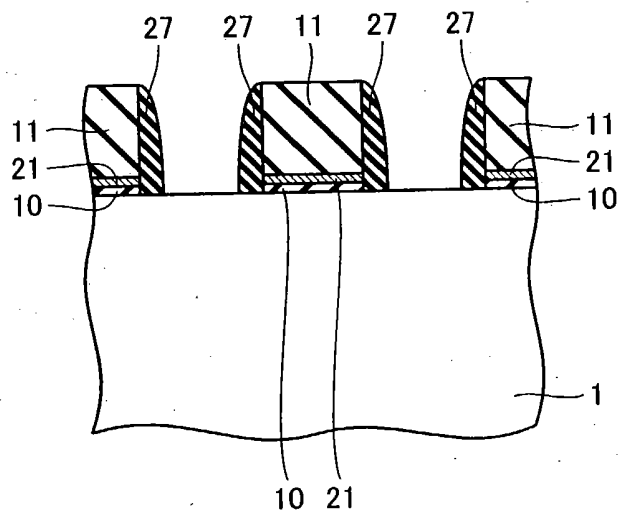


FIG.45

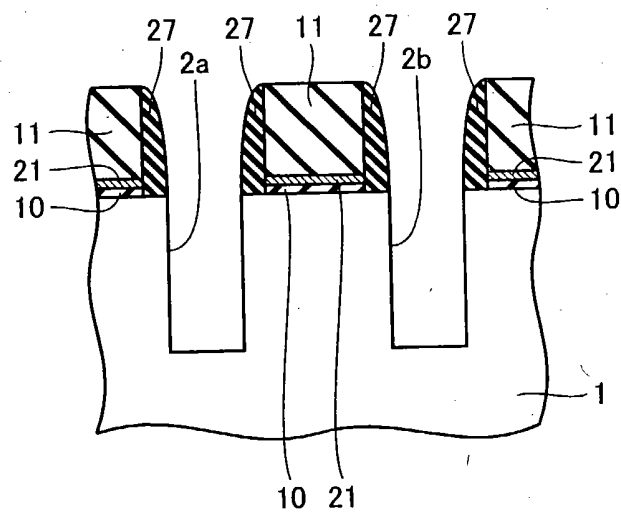


FIG.46

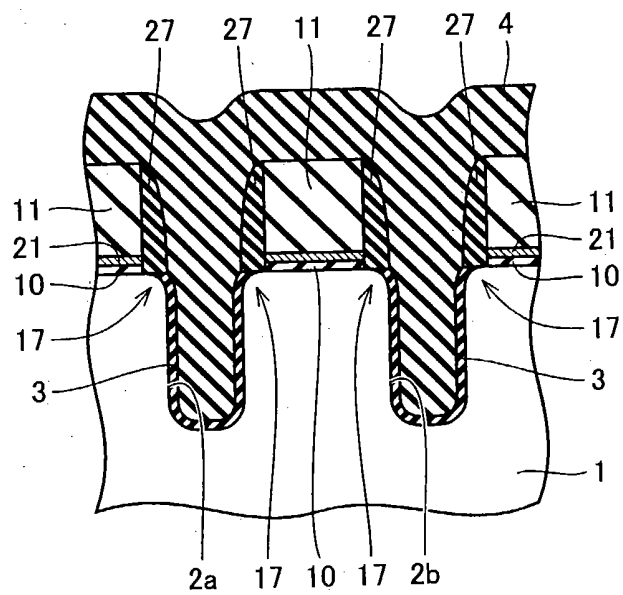




FIG.47

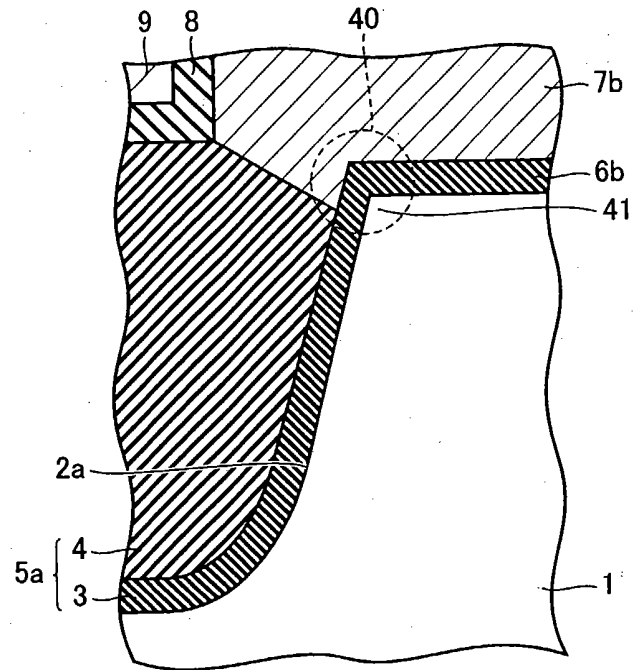


FIG.48

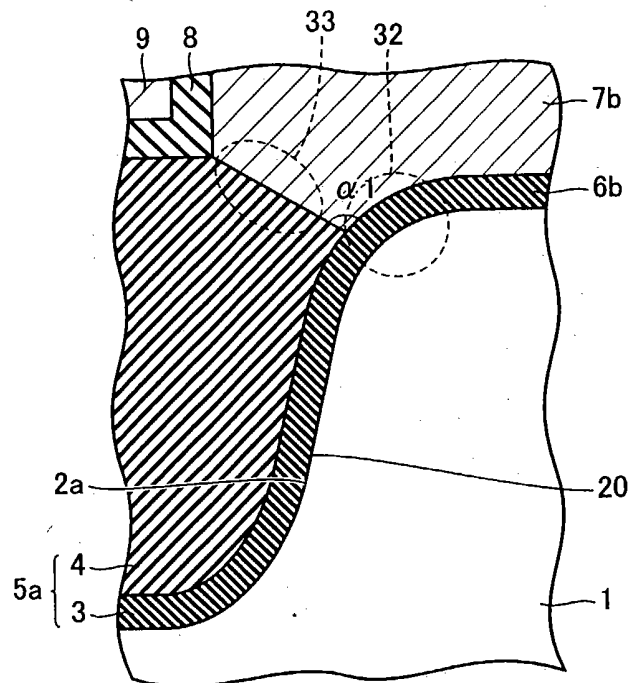


FIG.49

